

On the C11 Memory Model and a Program Logic for C11 Concurrency

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Topics

1 Motivation

2 C11

- Memory Model
- Atomic Accesses

3 Logic

- The Hoare Triple
- Separation Logic
- Relaxed Separation Logic

4 Conclusion

Common Weakness Enumeration¹

“TOP 25 Most Dangerous Software Errors”

- (41) CWE-456: Missing Initialisation
- (40) CWE-825: Expired Pointer Dereference
- (36) CWE-476: NULL Pointer Dereference
- (33) CWE-362: Concurrent Execution using Shared Resource with Improper Synchronisation ('Race Condition')

```
int init = 1;
int uninit;
int result
    = init + uninit;
```

¹http://cwe.mitre.org/top25/archive/2011/2011_onthecusp.html

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```
free(p);  
*p = 47;
```

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```
p = malloc(sizeof(int));  
    // out of memory !  
*p = 42;
```

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```
tmp = shared;
tmp = tmp&1
      ? 3*tmp +1
      : tmp>>1;
shared = tmp;
```

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Hidden Races

```
int data = 0;
```

```
void worker() {  
    for(int i=0; i < N; i++) {  
        data++;  
    }  
}
```

```
int main(..) {  
    pardo [worker() worker()] and join;  
    printf("data=%d", data);  
}
```

Hidden Races

```
void worker() { // gcc -00
    for(int i=0; i < N; i++) {
        register int tmp = data; // RAM: expensive
        tmp++;
        data = tmp;             // RAM: expensive
    }
}
```

```
void worker() { // gcc -01
    register int tmp = data;
    for(int i=0; i < N; i++)
        tmp++;

    data = tmp;
}
```

```
void worker() { // gcc -03
    register int tmp = data;
    tmp += N;
    data = tmp;
}
```


Situation until now

- C99/C0X standard: purely sequential
- Thread and synchronisation support via libraries (PThread, TBB, MS Windows Runtime Lib, C++/BOOST, ...)
- Limited compiler support
 - ▶ Optimisation unsound in concurrent programs?
 - ▶ Synchronisation inefficient (`__sync()` in GCC)

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Some Extensions of C11

- **Optional concurrency mode**
- Threads via `threads.h`
similar to POSIX threads (thread management, mutex, barrier)
- Atomic Memory Access via `stdatomic.h`
- Memory Model!

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C11 Memory Model

- Extends existing “evaluation rules”
- Allow compiler and processor as many optimisations as possible
- Support for
 - ▶ Sequential consistency
 - ▶ Acquire-Release
 - ▶ Consume-Release
 - ▶ Relaxed (just atomic)

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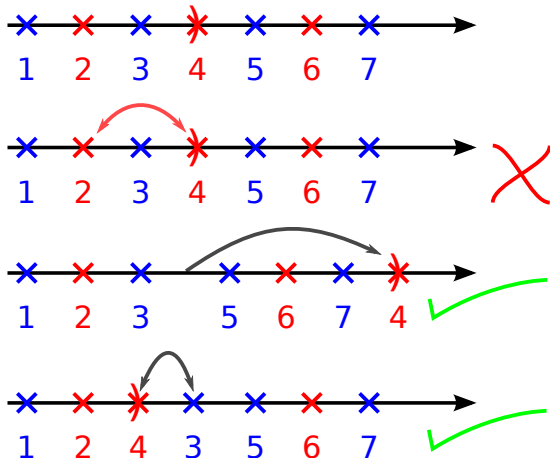
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Acquire-Release

load store

- All effects of instructions preceding a release R have to be observable before R
- All reads succeeding an acquire A have to happen after A
- Very efficient on x86 (plain reads/writes)



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```
v ← alloc();
r ← alloc();
f ← alloc(); [f]rlx ← 0;
( [v]na ← 47 ) ||| ( repeat [f]acq end )
( [f]rel ← 1 ) ||| ( r ← [v]na )
```

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stdatomic.h

- `atomic_load`, `-store`
- `atomic_fetch_add`, `-sub`,
`-or`, `-xor`, `-and`
- `atomic_exchange`
- `atomic_compare_exchange_weak`,
`-strong`
- `atomic_flag_clear`,
`-test_and_set ...`

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```
for(int i=0; i<N; i++) {  
    // data++;  
    atomic_fetch_add(&data, 1);  
}
```

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```
atomic_exchange(*p, val){  
    old = *p;  
  
    *p = val;  
    return old;  
}
```


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```
atomic_compare_exchange(*p,ref,val){
    old = *p;
    if (old == ref) {
        *p = val;
        return true;
    }

    return false;
}

spinlock(*p, threadId) {
    while(at_com_xchg_weak(
        p, 0, threadId));
}
```

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Program Logics

The Hoare Triple

$$(P) \{Q\} (R)$$

If the assertion P is true before [the] initiation of a program Q ,
then the assertion R will be true on its completion
[if the program terminates].

$$(x \mapsto 1) \{x \leftarrow x + 1\} (x \mapsto 2)$$

$$(x \mapsto 1) \{\text{while}(\text{true});\} (x \mapsto 2)$$

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Hoare Logic: “Rule of Composition”

$$\frac{(P) \{Q_1\} (R) \quad (R) \{Q_2\} (T)}{(P) \{Q_1; Q_2\} (T)}$$

$$\frac{(x \mapsto 1) \{x \leftarrow x + 1\} (x \mapsto 2) \quad (x \mapsto 2) \{y \leftarrow x\} (x \mapsto 2 \wedge y \mapsto 2)}{(x \mapsto 1) \{x \leftarrow x + 1; y \leftarrow x\} (x \mapsto 2 \wedge y \mapsto 2)}$$

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$$\frac{(P) \{Q_1\} (R) \quad (R) \{Q_2\} (T)}{(P) \{Q_1; Q_2\} (T)}$$

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Separation Logic

- Targets shared data structures (pointers, references)
- Efficient fully-automated verifier
- Distinguishes between
 - ▶ *Registers* represented by the Stack
 $s : \text{Vars} \mapsto \text{Values}$ with $\text{dom}(s) < \infty$
 - ▶ *Addressable Memory* represented by the Heap
 $h : \text{Addresses} \mapsto \text{Values}$ with $\text{dom}(h) < \infty$
- Separates independent code sections using the separation conjunction *

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Separation Logic: “Framing Rule”

$$\frac{(p) \{Q_1\} (q)}{(p * r) \{Q_1\} (q * r)}$$

$$(x \neq y \wedge (x \mapsto 2 * y \mapsto 2)) \{[x] \leftarrow 3\} (x \mapsto 3 * y \mapsto 2)$$

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$$(x \neq y \wedge (x \mapsto 2 * y \mapsto 2)) \{[x] \leftarrow 3\} (x \mapsto 3 * y \mapsto 2)$$

$$(x = y \wedge (x \mapsto 2 * y \mapsto 2)) \{[x] \leftarrow 3\} (x \mapsto 3 * y \mapsto 2)$$

Separation Logic: “Framing Rule”

$$\frac{(p) \{Q_1\} (q)}{(p * r) \{Q_1\} (q * r)}$$

$$(x \neq y \wedge (x \mapsto 2 * y \mapsto 2)) \{[x] \leftarrow 3\} (x \mapsto 3 * y \mapsto 2)$$

~~$$(x = y \wedge (x \mapsto 2 * y \mapsto 2)) \{[x] \leftarrow 3\} (x \mapsto 3 * y \mapsto 2)$$~~

Relaxed Separation Logic

- A (complete) C-language subset
- Rules to infer a Hoare-Triple annotation
- Central Theorem (Coq-proven):
If annotation is successful \Rightarrow program is memory sound

Relaxed Separation Logic

$$P, Q := \underbrace{\mathbf{false} \mid P \Rightarrow Q \mid \forall x. P}_{\text{complete first order logic}} \mid \underbrace{\mathbf{emp} \mid e \xrightarrow{k} e' \mid P * Q}_{\text{known from SL}} \\ \mid \mathit{Rel}(e, \mathcal{Q}) \mid \mathit{Acq}(e, \mathcal{Q}) \mid \mathit{RMWAcq}(e, \mathcal{Q}) \\ \mid \mathit{Init}(e) \mid \mathit{Uinit}(e)$$

Relaxed Separation Logic

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Relaxed Separation Logic

(emp)

$v \leftarrow \text{alloc}(); r \leftarrow \text{alloc}();$

$f \leftarrow \text{alloc}();$

$[f]_{\text{rlx}} \leftarrow 0;$

$\left(\begin{array}{l} [v]_{\text{na}} \leftarrow 47 \\ [f]_{\text{rel}} \leftarrow 1 \end{array} \right) \parallel \left(\begin{array}{l} \text{repeat } [f]_{\text{acq}} \text{ end} \\ [r]_{\text{na}} \leftarrow [v]_{\text{na}} \end{array} \right)$

Relaxed Separation Logic

(emp)

$v \leftarrow \text{alloc}(); r \leftarrow \text{alloc}();$

$(\text{Uninit}(v) * \text{Uninit}(r))$

$f \leftarrow \text{alloc}();$

$[f]_{\text{rlx}} \leftarrow 0;$

$\left(\begin{array}{l} [v]_{\text{na}} \leftarrow 47 \\ [f]_{\text{rel}} \leftarrow 1 \end{array} \right) \parallel \left(\begin{array}{l} \text{repeat } [f]_{\text{acq}} \text{ end} \\ [r]_{\text{na}} \leftarrow [v]_{\text{na}} \end{array} \right)$

Non-Atomic Allocation

(emp) { alloc() } (x. Uninit(x))

Relaxed Separation Logic

$$\begin{aligned} &v \leftarrow \text{alloc}(); \quad r \leftarrow \text{alloc}(); \\ &\quad (\text{Uninit}(v) * \text{Uninit}(r)) \\ &\quad \quad f \leftarrow \text{alloc}(); \\ &(\text{Uninit}(v) * \text{Uninit}(r) * \text{Rel}(f, \mathcal{Q}) * \text{Acq}(f, \mathcal{Q})) \\ &\quad \quad [f]_{\text{rlx}} \leftarrow 0; \\ &\left(\begin{array}{l} [v]_{\text{na}} \leftarrow 47 \\ [f]_{\text{rel}} \leftarrow 1 \end{array} \right) \parallel \left(\begin{array}{l} \mathbf{repeat} [f]_{\text{acq}} \mathbf{end} \\ [r]_{\text{na}} \leftarrow [v]_{\text{na}} \end{array} \right) \end{aligned}$$

Atomic Allocation

$$(\mathbf{emp}) \{ \text{alloc}() \} (x. \text{Rel}(x, \mathcal{Q}) * \text{Acq}(x, \mathcal{Q}))$$

Relaxed Separation Logic

$$\begin{aligned} &v \leftarrow \text{alloc}(); \quad r \leftarrow \text{alloc}(); \\ &\quad f \leftarrow \text{alloc}(); \\ &(\text{Uninit}(v) * \text{Uninit}(r) * \text{Rel}(f, \mathcal{Q}) * \text{Acq}(f, \mathcal{Q})) \\ &\quad [f]_{\text{rlx}} \leftarrow 0; \\ &(\text{Uninit}(v) * \text{Uninit}(r) * \text{Rel}(f, \mathcal{Q}) * \text{Acq}(f, \mathcal{Q}) * \text{Init}(f)) \\ &\quad \left(\begin{array}{l} [v]_{\text{na}} \leftarrow 47 \\ [f]_{\text{rel}} \leftarrow 1 \end{array} \right) \parallel \left(\begin{array}{l} \text{repeat } [f]_{\text{acq}} \text{ end} \\ [r]_{\text{na}} \leftarrow [v]_{\text{na}} \end{array} \right) \end{aligned}$$

Relaxed Write (simplified)

$$(\text{Rel}(\cdot)) \{ [l] \leftarrow v \} (\text{Init}(l))$$

Relaxed Separation Logic

$v \leftarrow \text{alloc}(); r \leftarrow \text{alloc}();$

$f \leftarrow \text{alloc}();$

$[f]_{\text{rlx}} \leftarrow 0;$

$(\text{Uninit}(v) * \text{Uninit}(r) * \text{Rel}(f, Q) * \text{Acq}(f, Q) * \text{Init}(f))$

$$\left(\begin{array}{l} (\text{Uninit}(v) * \text{Rel}(f, Q)) \\ [v]_{\text{na}} \leftarrow 47 \\ [f]_{\text{rel}} \leftarrow 1 \end{array} \right) \parallel \left(\begin{array}{l} (\text{Uninit}(r) * \text{Acq}(f, Q) * \text{Init}(f)) \\ \text{repeat } [f]_{\text{acq}} \text{ end} \\ [r]_{\text{na}} \leftarrow [v]_{\text{na}} \end{array} \right)$$

Parallel Composition

$$\frac{(P_1) \{Q_1\} (R_1) \quad (P_2) \{Q_2\} (R_2)}{(P_1 * P_2) \{Q_1 \parallel Q_2\} (R_1 * R_2)}$$

Relaxed Separation Logic

$v \leftarrow \text{alloc}(); r \leftarrow \text{alloc}();$

$f \leftarrow \text{alloc}();$

$[f]_{\text{rlx}} \leftarrow 0;$

$$\left(\begin{array}{l} (\text{Uninit}(v) * \text{Rel}(f, \mathcal{Q})) \\ [v]_{\text{na}} \leftarrow 47 \\ (v \mapsto 47 * \text{Rel}(f, \mathcal{Q})) \\ [f]_{\text{rel}} \leftarrow 1 \end{array} \right) \parallel \parallel \left(\begin{array}{l} (\text{Uninit}(r) * \text{Acq}(f, \mathcal{Q}) * \text{Init}(f)) \\ \text{repeat } [f]_{\text{acq}} \text{ end} \\ [r]_{\text{na}} \leftarrow [v]_{\text{na}} \end{array} \right)$$

Non-Atomic Write

$$(I \stackrel{1}{\mapsto} _ \vee \text{Uninit}(I)) \{ [I]_{\text{na}} \leftarrow v \} (I \stackrel{1}{\mapsto} v)$$

Relaxed Separation Logic

$v \leftarrow \text{alloc}(); r \leftarrow \text{alloc}();$

$f \leftarrow \text{alloc}();$

$[f]_{\text{rlx}} \leftarrow 0;$

$$\left(\begin{array}{l} [v]_{\text{na}} \leftarrow 47 \\ \underbrace{(v \mapsto 47 * \text{Rel}(f, Q))}_Q \\ [f]_{\text{rel}} \leftarrow 1 \\ (\text{Rel}(f, Q)) \end{array} \right) \parallel \left(\begin{array}{l} (\text{Uninit}(r) * \text{Acq}(f, Q) * \text{Init}(f)) \\ \text{repeat } [f]_{\text{acq}} \text{ end} \\ [r]_{\text{na}} \leftarrow [v]_{\text{na}} \end{array} \right)$$

Atomic Write

$$(Q(v) * \text{Rel}(l, Q)) \{ [l]_{\text{rel}} \leftarrow v \} (\text{Init}(l) * \text{Rel}(l, Q))$$

Relaxed Separation Logic

$$\begin{array}{l} v \leftarrow \text{alloc}(); \ r \leftarrow \text{alloc}(); \\ f \leftarrow \text{alloc}(); \\ [f]_{\text{rlx}} \leftarrow 0; \end{array} \quad \left\| \quad \begin{array}{l} (\text{Uninit}(r) * \text{Acq}(f, Q) * \text{Init}(f)) \\ \text{repeat } [f]_{\text{acq}} \text{ end} \\ \underbrace{(v \xrightarrow{1} 47 * \text{Uninit}(r) * \text{true})}_Q \\ [r]_{\text{na}} \leftarrow [v]_{\text{na}} \end{array} \right)$$

Atomic Read (simplified)

$$(\text{Init}(l) * \text{Acq}(l, Q)) \{ [l]_{\text{acq}} \} (v.Q(v) * \text{Acq}(\dots))$$

Relaxed Separation Logic

$$\begin{array}{l} v \leftarrow \text{alloc}(); \ r \leftarrow \text{alloc}(); \\ f \leftarrow \text{alloc}(); \\ [f]_{\text{rlx}} \leftarrow 0; \\ \left(\begin{array}{l} [v]_{\text{na}} \leftarrow 47 \\ [f]_{\text{rel}} \leftarrow 1 \end{array} \right) \parallel \left(\begin{array}{l} \text{repeat } [f]_{\text{acq}} \text{ end} \\ \underbrace{(v \xrightarrow{1} 47 * \text{Uunit}(r) * \text{true})}_Q \\ [r]_{\text{na}} \leftarrow [v]_{\text{na}} \\ (\text{true} * r \mapsto 47 * v \mapsto 47) \end{array} \right) \end{array}$$

Non-Atomic Read

$$(l \xrightarrow{k} v) \{ [l]_{\text{na}} \} (x.x = v \wedge l \xrightarrow{k} v)$$

Relaxed Separation Logic

$$\begin{array}{l} v \leftarrow \text{alloc}(); \ r \leftarrow \text{alloc}(); \\ f \leftarrow \text{alloc}(); \\ [f]_{\text{rlx}} \leftarrow 0; \\ \left(\begin{array}{l} [v]_{\text{na}} \leftarrow 47 \\ [f]_{\text{rel}} \leftarrow 1 \\ (\text{Rel}(f, Q)) \end{array} \right) \parallel \left(\begin{array}{l} \text{repeat } [f]_{\text{acq}} \text{ end} \\ [r]_{\text{na}} \leftarrow [v]_{\text{na}} \\ (\text{true} * r \mapsto 47 * v \mapsto 47) \end{array} \right) \\ (\text{true} * r \mapsto 47) \end{array}$$

Parallel Composition

$$\frac{(P_1) \{Q_1\} (R_1) \quad (P_2) \{Q_2\} (R_2)}{(P_1 * P_2) \{Q_1 \parallel Q_2\} (R_1 * R_2)}$$

Conclusion & Outlook

- C11 is now officially fit for concurrent programs
- RSL shows how to perform formal arguments on (subset) of C11-MM
- Fully automated verifier?

Thank you for your attention!
Questions?

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